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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,754	08/18/2000	In Sung Kim	SEC.747	7644

7590 04/02/2002

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EXAMINER
COLLINS, DEVEN M

ART UNIT	PAPER NUMBER
2823	9

DATE MAILED: 04/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/640,754	KIM ET AL.	
	Examiner	Art Unit	
	D. M. Collins	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,14,15 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,14,15 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 1 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-10, 14-15, and 21-23 are rejected under 35 U.S.C. 102(e) as being unpatentable over Lee et al. (6,136,695, dated 10/24/00).

Lee et. al. show the method e as claimed in the Figures 1-3 with corresponding text. In re claim 1, Lee et al. disclose a method of fabricating a semiconductor device, comprising:

forming a conductive region 25 at the top of a semiconductor substrate 10;

forming a first interlayer dielectric layer 60 on the semiconductor substrate 10 over the entirety of the conductive region 25;

forming a conductive line 20, which is to be connected to the conductive region 25, on the first interlayer dielectric layer 60;

forming a second interlayer dielectric layer 70 on the conductive line 20;

removing portions of the first interlayer dielectric layer 60, conductive line 20, and second interlayer dielectric layer 70 which overlie the conductive region 25 to form a contact hole 55 which exposes the conductive region 25; and

filling the contact hole 55 with a conductive material to connect the conductive line 20 to the conductive region 25.

In re claim 2, Lee et al. disclose the method of claim 1, wherein said removing of portions of the first interlayer dielectric layer 60, conductive line 20, and second interlayer dielectric layer 70 comprises: forming a patterned photosensitive film on the second interlayer dielectric layer 70, the patterned photosensitive film defining an opening therein having a width that is greater than the critical dimension of the conductive line 20, etching (col. 3, line 58) the second interlayer dielectric layer 70 using the photosensitive film pattern as an etch mask 30 until the conductive line 20 is exposed, and etching (col. 3, line 58) the conductive line 20 and the first interlayer dielectric layer 60 using the etched second interlayer dielectric layer 70 as an etch mask 30.

In re claim 3, Lee et al. disclose the method of claim 2, wherein the etching of the conductive line 20 and the first interlayer dielectric layer 60 comprises:
etching (col.3, line 58) the conductive line 20 using the etched second interlayer dielectric layer 70 as an etch mask 30 to expose the first interlayer dielectric layer 60, and then discretely etching the exposed first interlayer dielectric layer 60.

In re claim 4, Lee et al. disclose the method of claim 2, wherein the etching of the second interlayer dielectric layer 60 comprises an anisotropic etching (col. 3, line 58) process which produces inclined sidewalls 40a therein, whereby the cross-sectional area of an upper portion of the contact hole 55 is greateer than that of a lower portion thereof.

In re claim 5, Lee et al. disclose the method of claim 3, wherein the etching of the second interlayer dielectric layer 70 comprises an anisotropic etching process which produces inclined sidewalls 40a therein, whereby the cross-sectional area of an upper portion of the contact hole 55 is greater than that of a lower portion thereof.

In re claim 6, Lee et al. disclose the method of claim 2, and further comprising removing the photosensitive film pattern before the conductive line 20 is etched.

In re claim 7, Lee et al. disclose the method of claim 3, and further comprising removing the photosensitive film pattern before the conductive line 20 is etched.

In re claim 8, Lee et al. disclose the method of claim 1, wherein the forming of the conductive line 20 comprises:

forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer 60, and

depositing conductive material in the line-shaped opening.

In re claim 9, Lee et al. disclose a method of fabricating semiconductor devices, comprising:

forming a conductive region 25 at the top of a semiconductor substrate 10;

forming a first interlayer dielectric layer 60 on the semiconductor substrate 10 over the entirety of the conductive region 25;

forming a conductive line 20, which is to be connected to the conductive region 25, on the first interlayer dielectric layer 60, the conductive line 20 having a gap therein of a predetermined width;

forming a second interlayer dielectric layer 70 on the conductive line 20 such that a first 60 portion of the second interlayer dielectric layer 70 occupies the gap in the conductive line 20;

removing a portion of the first interlayer dielectric layer 60 overlying the conductive region, the first portion of the second interlayer dielectric layer occupying the gap in the conductive line 20, and a second portion of the second interlayer dielectric layer overlying the gap to form a contact hole 55; and

filling the contact hole 55 with a conductive material to connect the conductive line 20 to the conductive region 25.

In re claim 10, Lee et al. disclose the method of claim 9, wherein the of removihg portions of the first 60 and second interlayer dielectric layers 70 comprises:

forming a photosensitive film pattern on the second interlayer dielectric layer, the photosensitive film pattern defining an opening therein having widths, in two orthogonal X and Y directions, that are greater than the critical dimension of and the width of the gap in the conductive line 20, respectively, and

etching the second portion of the second interlayer dielectric layer , the first portion of the second interlayer dielectric layer occupying the gap in the conductive line 20, and a portion of the first interlayer dielectric layer underlying the gap in the conductive line 20, using the photosensitive film pattern and the conductive line 20 as etch masks 30.

In re claim 14, Lee et al. disclose the method of claim 21, further comprising removing the photosensitive film pattern after the portion of the conductive line 20 defining the gap therein is exposed.

In re claim 15, Lee et al. disclose the method of claim 9, wherein the forming of the conductive line 20 comprises:

forming a dielectric film pattern having a line-shaped opening on the first

interlayer dielectric layer 60; and depositing conductive material within the line-shaped opening.

In the claim 21, Lee et al. disclose the method of claim 10, wherein the etching of the first and second interlayer dielectric layers comprises:

etching the second portion of the second interlayer dielectric layer 70 using the photosensitive film pattern as an etch mask 30 until a portion of the conductive line 20 defining the gap is exposed, and etching the first portion of the second interlayer dielectric layer occupying the gap in the conductive line 20, and the portion of the first interlayer dielectric layer underlying the

gap, using the etched second interlayer dielectric layer and the portion of the conductive line defining the gap therein as etch masks 30.

In the claim 22, Lee et al. disclose the method of claim 10, wherein the etching of the portion of the first portion of the second interlayer dielectric layer occupying the gap in the conductive line 20 comprises an anisotropic etching process which produces inclined sidewalls in the conductive line 20, whereby the cross-sectional area of an upper portion of the contact hole 55 is greater than that of a lower portion thereof.

In the claim 23, Lee et al. disclose the method of claim 21, wherein the etching of the portion of the first portion of the second interlayer dielectric layer occupying the gap in the conductive line 20 comprises an anisotropic etching process which produces inclined sidewalls in the conductive line 20, whereby the cross-sectional area of an upper portion of the contact hole 55 is greater than that of a lower portion thereof.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Deven M. Collins whose telephone number is (703) 305-7840. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy, can be reached on (703) 308-4918. The fax phone number for this Group is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

DMC

March 22, 2002

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800